ABSTRACT OF THE DISCLOSURE

A method for verifying optimization of processor link. First, an initial bus width and an initial bus frequency of a bus coupled between a CPU and a Northbridge are set, such that the bus operates at the initial bus width and the initial bus frequency. Next, a read request for a Southbridge is generated. Next, a bus disconnection signal is output by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receives the read request. A timer is initialized for calculating an elapsed time value and an optimization verification signal at a first voltage level is generated. Next, a bus connection signal is output by the Southbridge when the elapsed time value reaches a predetermined value. Next, the voltage level of the optimization verification signal is transformed to a second voltage level. Finally, the CPU and the Northbridge are reconnected by the bus according to the bus connection signal, such that the bus operates at another bus operating bus width and another bus operating frequency.